WHAT IS CLAIMED IS:

1. A method for isolating degradation mechanisms in transistors comprising:

providing a ring oscillator having a plurality of delay elements, each delay element operating as a delay element through the use of one or more transistors of only a first type and no transistors of the opposite type;

operating the ring oscillator and measuring the frequency resulting from the oscillator over time; and

determining the magnitude of an isolated degradation mechanism based on a comparison of the measured frequency and an expected frequency for the ring oscillator absent degradation.

2. The method of Claim 1, wherein the first type is an NMOS transistor and the isolated degradation mechanism is NMOS CHC degradation.

3. The method of Claim 1, wherein the first type is a PMOS transistor and the isolated degradation mechanism is PMOS degradation.

4. The method of Claim 1, wherein the delay elements each comprise an inverter formed from a resister in series with an NMOS transistor and the gate at the NMOS transistor is coupled to an output of a preceding delay element in the ring oscillator.

5. The method of Claim 1, wherein the delay elements each comprise an inverter formed from first and second NMOS transistors connected together in series with the gate of the first transistor coupled to the drain of the first transistor and the gate of the second transistor coupled to an output of a preceding delay element in the ring oscillator.

6. The method of Claim 1, wherein the delay elements each comprise an inverter formed from a resister in series with a PMOS transistor and the gate of the PMOS transistor is coupled to an output of a preceding delay element in the ring oscillator.

7. The method of Claim 2, wherein each of the delay elements is an inverter.

8. The method of Claim 3, wherein each of the delay elements is an inverter.

9. The method of Claim 3, wherein the one or more transistors each comprise gates greater than or equal to one micron in length.

10. The method of Claim 3, where the one or more transistors each comprise gates less than or equal to 0.1 microns in length.

11. A method of isolating degradation mechanisms in transistors comprising:

providing first and second ring oscillators each having a plurality of delay elements, each delay element operating as a delay element through the use of one or more PMOS transistors and no NMOS transistors, the PMOS transistors in the first ring oscillator having a gate length greater than or equal to about one micron and the PMOS transistors in the second ring oscillator having a gate length of less than or equal to about 0.1 microns;

operating the first and second ring oscillators and measuring their respective frequencies resulting from the respective oscillators over time;

determining, based on simulation of the first ring oscillator and the measured frequency over time of the first ring oscillator, a degradation component associated with NBTI PMOS degradation;

using the determined NBTI PMOS degradation, modeling the operation of the second ring oscillator to match the measured frequency over time characteristics of the second ring oscillator; and

based on the model of the second ring oscillator, determining a degradation component associated with CHC PMOS degradation.

12. The method of Claim 11, wherein the delay elements in each of the ring oscillators each comprise inverters.

13. The method of Claim 12, wherein the inverters in each of the ring oscillators each comprise a PMOS transistor connected in series with a resister and having a gate connected to an output of a preceding inverter in the respective ring oscillator.

14. The method of Claim 11, wherein modeling the operation of the second ring oscillator comprises modeling the second ring oscillator with the HOTRON software program.

15. A system for determining degradation components in a transistor comprising:

a ring oscillator comprising a plurality of delay elements each comprising at least one transistor for which the degradation component is described and having a gate length of less than or equal to about 0.1 microns;

a frequency counter operable to measure the frequency of the ring oscillator over time; and

wherein each of the delay elements comprises no transistors of a type opposite to the type of the at least one transistor.

16. The system of Claim 15, and wherein the at least one transistor is an PMOS transistor.

17. The system of Claim 15, and wherein the at least one transistor is an NMOS transistor.

18. The system of Claim 15, wherein each delay element is an inverter.

19. The system of Claim 18, wherein each delay element comprises a resistor in series with the at least one transistor and wherein the at least one transistor comprises a gate connected to an output of a preceding inverter in the ring oscillator.

20. The system of Claim 18, wherein the at least one transistor comprises first and second transistors connected in series, the first transistor having a gate connected to an output of a preceding inverter in the ring oscillator and the second transistor having a drain and a gate coupled together.

METHOD AND SYSTEM FOR DETERMINING
TRANSISTOR DEGRADATION MECHANISMS